BURR-BROWN®

INA110

Fast-Settling FET-Input Very High Accuracy INSTRUMENTATION AMPLIFIER

FEATURES

- LOW BIAS CURRENT: 50pA, max
- FAST SETTLING: 4μs to 0.01%
- HIGH CMR: 106dB, min; 90dB at 10kHz
- CONVENIENT INTERNAL GAINS: 1, 10, 100, 200, 500
- VERY-LOW GAIN DRIFT: 10 to 50ppm/°C
- LOW OFFSET DRIFT: 2μV/°C
- LOW COST
- PINOUT COMPATIBLE WITH AD524 AND AD624, allowing upgrading of many existing applications

APPLICATIONS

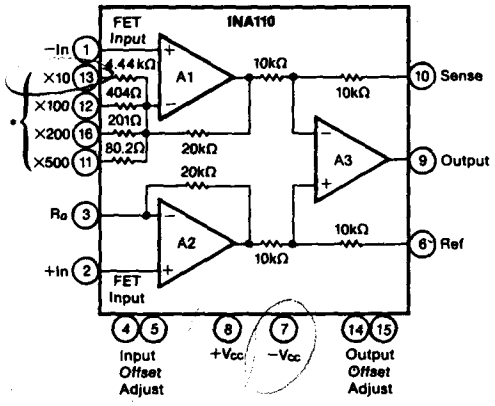
- Fast scanning rate multiplexed input data acquisition system amplifier
- Fast differential pulse amplifier
- High speed, low drift gain block
- Amplification of low level signals from high impedance sources and sensors
- Instrumentation amplifier with input low pass filtering using large series resistors
- Instrumentation amplifier with overvoltage input protection using large series resistors
- Amplification of signals from strain gauges, thermocouples, and RTDs

DESCRIPTION

The INA110 is a monolithic FET input instrumentation amplifier with a maximum bias current of 50pA. The circuit provides fast settling of 4μs to 0.01%. Laser trimming guarantees exceptionally good DC performance. Voltage noise is low, and current noise is virtually zero. Internal gain set resistors guarantee high gain accuracy and low gain drift. Gains of 1, 10, 100, 200, and 500 are provided.

The inputs are inherently protected by P-channel FETs on each input. Differential and common-mode voltages should be limited to ±Vcc. When severe overvoltage exists, use diode clamps as shown in the application section.

The INA110 is ideally suited for applications requiring large input resistors for overvoltage protection or filtering. Input signals from high source impedances can easily be handled without degrading DC performance. Fast settling for rapid scanning data acquisition systems is now achievable with one component, the INA110.



* Connect to Rα for desired gain.

International Airport Industrial Park - P.O. Box 11400 - Tucson, Arizona 85734 - Tel. (602) 746-1111 - Twx: 910-952-1111 - Cable: BBRCORP - Telex: 66-6491

NA110

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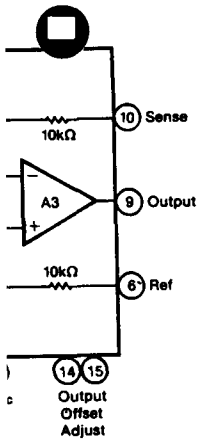


ı gain.

: BBRCORP - Telex: 66-6491

SPECIFICATIONS

ELECTRICAL

At +25°C, ±V_{CC} = 15VDC, R_L = 2kΩ unless otherwise noted.

PARAMETER	CONDITIONS	INA110AG MIN	INA110AG TYP	INA110AG MAX	INA110BG MIN	INA110BG TYP	INA110BG MAX	UNITS
GAIN								
Range of Gain		1		800	•		•	V/V
Gain Equation[1]				G = 1 + [40K/(R_G + 50Ω)]				V/V
Gain Error, DC: G = 1			0.002	0.04		•	0.02	%
G = 10			0.01	0.1		0.005	0.05	%
G = 100			0.02	0.2		0.01	0.1	%
G = 200			0.04	0.4		0.02	0.2	%
G = 500			0.1	1.0		0.05	0.5	%
Gain Temp. Coefficient: G = 1			±3	±20		•	±10	ppm/°C
G = 10			±4	±20		±2	±10	ppm/°C
G = 100			±6	±40		±3	±20	ppm/°C
G = 200			±10	±60		±5	±30	ppm/°C
G = 500			±25	±100		±10	±50	ppm/°C
Nonlinearity, DC: G = 1			±0.001	±0.01		±0.0005	±0.005	% of FS
G = 10			±0.002	±0.01		±0.001	±0.005	% of FS
G = 100			±0.004	±0.02		±0.002	±0.01	% of FS
G = 200			±0.006	±0.02		±0.003	±0.01	% of FS
G = 500			±0.01	±0.04		±0.005	±0.02	% of FS
OUTPUT								
Voltage, R_L = 2kΩ	Over temp	±10	±12.7		•	•		V
Current	Over temp	±5	±25		•	•		mA
Short-Circuit Current			±25			•		mA
Capacitive Load	Stability		5000			•		pF
INPUT								
OFFSET VOLTAGE[2]								
Initial Offset			±(100+1000/G)	±(500+5000/G)		±(50+600/G)	±(250+3000/G)	µV
vs Temperature			±(2+20/G)	±(5+100/G)		±(1+10/G)	±(2+50/G)	µV/°C
vs Supply	V_{CC} = ±6V to ±18V		±(4+60/G)	±(30+300/G)		±(2+30/G)	±(10+180/G)	µV/V
BIAS CURRENT								
Initial Bias Current	Each input		20	100		10	50	pA
Initial Offset Current			2	50		1	25	pA
Impedance: Differential			$5X10^{12}$‖6			•		Ω‖pF
Common-Mode			$2X10^{12}$‖1			•		Ω‖pF
VOLTAGE RANGE	V_{IN} Diff. = 0V[3]							
Range, Linear Response		±10	±12					V
CMR with 1kΩ Source Imbalance:								
G = 1	DC	70	90		80	100		dB
G = 10	DC	87	104		96	112		dB
G = 100	DC	100	110		106	116		dB
G = 200	DC	100	110		106	116		dB
G = 500	DC	100	110		106	116		dB
NOISE, Input[4]								
Voltage, f_O = 10kHz			10			•		nV/√Hz
f_B = 0.1Hz to 10Hz			1			•		µVp-p
Current, f_O = 10kHz			1.8			•		fA/√Hz
NOISE, Output[4]								
Voltage, f_O = 10kHz			65			•		nV/√Hz
f_B = 0.1Hz to 10Hz			8			•		µVp-p
DYNAMIC RESPONSE								
Small Signal: G = 1	−3dB		2.5			•		MHz
G = 10			2.5			•		MHz
G = 100			470			•		kHz
G = 200			240			•		kHz
G = 500			100			•		kHz
Full Power	V_{OUT} = ±10V, R_L = 2kΩ	190	270		•	•		kHz
Slew Rate	G = 1 to 200	12	17		•	•		V/µs
Settling Time:								
0.1%, G = 1	V_O = 20V step		4			•		µs
G = 10			2			•		µs
G = 100			3			•		µs
G = 200			5			•		µs
G = 500			11			•		µs

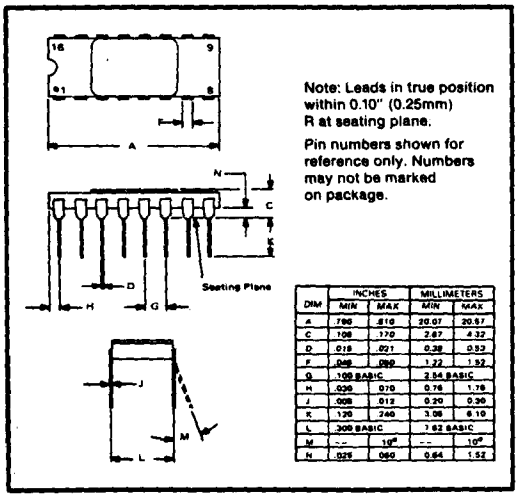
ELECTRICAL (CONT)

PARAMETER	CONDITIONS	INA110AG			INA110BG			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Settling Time:								
0.01%, G = 1	V_O = 20V step		5	12.5		•	•	µs
G = 10			3	7.5		•	•	µs
G = 100			4	7.5		•	•	µs
G = 200			7	12.5		•	•	µs
G = 500			16	25		•	•	µs
Overload Recovery[5]	50% overdrive		1			•		µs
POWER SUPPLY								
Rated Voltage			±15			•		V
Voltage Range		±6		±18	•		•	V
Quiescent Current	V_O = 0V		±3.0	±4.5		•	•	mA
TEMPERATURE RANGE								
Specification		−25		+85	•		•	°C
Operation		−55		+125	•		•	°C
Storage		−65		+150	•		•	°C
θ_{JA}			100			•		°C/W

* Same as INA110AG.

NOTES: (1) Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G, between pin 3 and pins 11, 12, and 16. Gain accuracy is a function of R_G and the internal resistors which have a ±20% tolerance with 20ppm/°C drift. (2) Adjustable to zero. (3) For differential input voltage other than zero, see Typical Performance Curves. (4) $V_{NOISE\ RTI} = \sqrt{V_{N\ INPUT}^2 + (V_{N\ OUTPUT}/Gain)^2}$. (5) Time required for output to return from saturation to linear operation following the removal of an input overdrive voltage.

MECHANICAL



Note: Leads in true position within 0.10" (0.25mm) R at seating plane.

Pin numbers shown for reference only. Numbers may not be marked on package.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.780	.810	20.07	20.57
C	.105	.170	2.67	4.32
D	.015	.021	0.38	0.53
F	.045	.060	1.22	1.52
G	.100 BASIC		2.54 BASIC	
H	.030	.070	0.76	1.78
J	.008	.012	0.20	0.30
K	.120	.240	3.08	6.10
L	.300 BASIC		7.62 BASIC	
M	--	10°	--	10°
N	.025	.060	0.64	1.52

PIN CONFIGURATION

−In	1	16	×200
+In	2	15	Output Offset Adjust
R_G	3	14	Output Offset Adjust
Input Offset Adjust	4	13	×10
Input Offset Adjust	5	12	×100
Reference	6	11	×500
$-V_{CC}$	7	10	Output Sense
$+V_{CC}$	8	9	Output

ORDERING INFORMATION

INA110 X G

Basic Model Number

Performance Grade Code
A, B: −25°C to +85°C

Package Code
G: 16-Pin Hermetic DIP

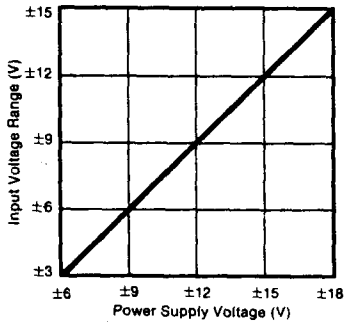
ABSOLUTE MAXIMUM RATINGS

Supply ..... ±18V
Input Voltage Range ..... $\pm V_{CC}$
Operating Temperature Range ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (soldering 10 seconds) ..... +300°C
Output Short-Circuit Duration ... Continuous to Common

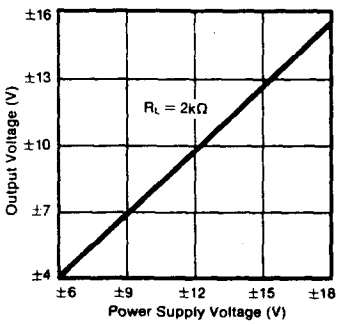
TYPICAL PERFORMANCE CURVES

T_A = 25°C, $\pm V_{CC}$ = 15VDC unless otherwise noted.

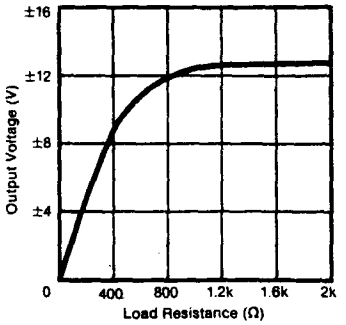
INPUT VOLTAGE RANGE VS SUPPLY



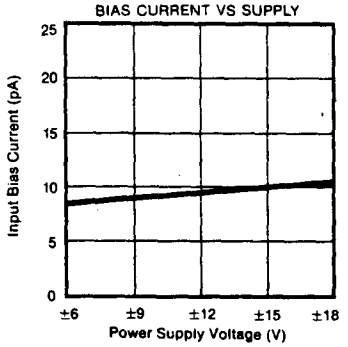
OUTPUT SWING VS SUPPLY



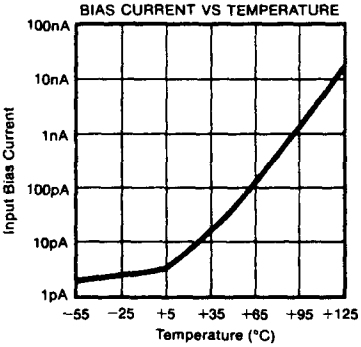
OUTPUT SWING VS LOAD RESISTANCE



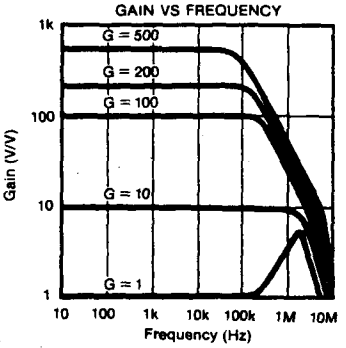
BIAS CURRENT VS SUPPLY



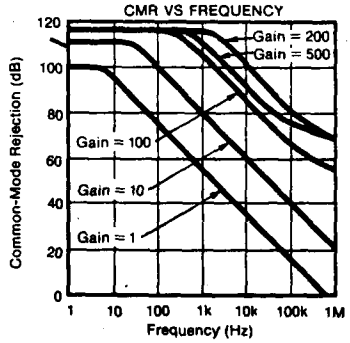
BIAS CURRENT VS TEMPERATURE



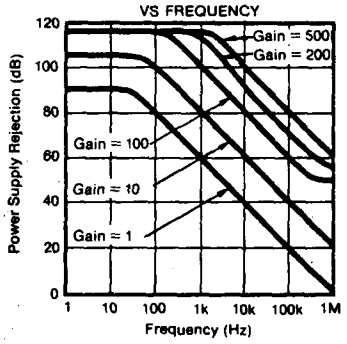
GAIN VS FREQUENCY



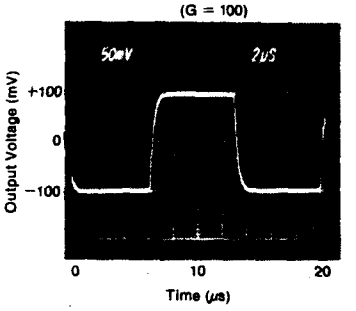
CMR VS FREQUENCY



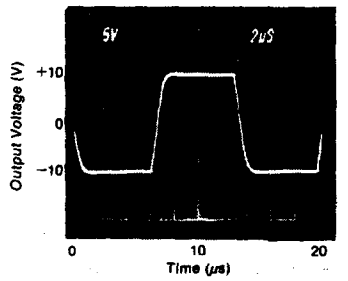
POWER SUPPLY REJECTION VS FREQUENCY



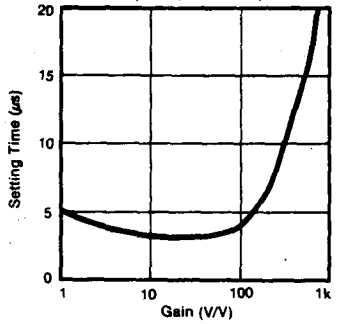
SMALL SIGNAL TRANSIENT RESPONSE (G = 100)



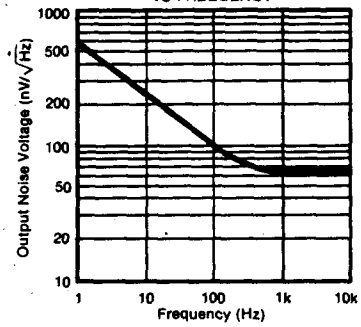
LARGE SIGNAL TRANSIENT RESPONSE (G = 100)



SETTLING TIME VS GAIN (0.01%, 20V STEP)



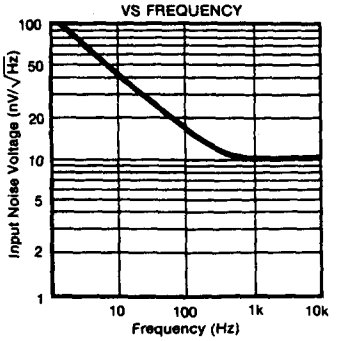
OUTPUT NOISE VOLTAGE VS FREQUENCY



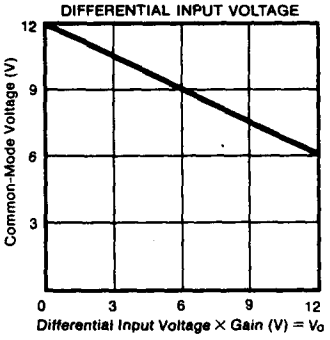
TYPICAL PERFORMANCE CURVES (CONT)

T_A = 25°C, ±V_{CC} = 15VDC unless otherwise noted.

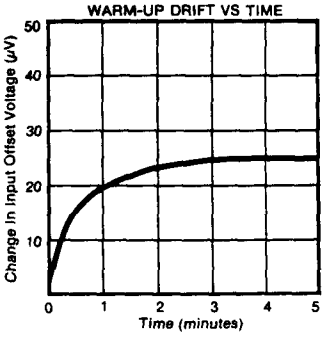
INPUT NOISE VOLTAGE VS FREQUENCY



COMMON-MODE VOLTAGE VS DIFFERENTIAL INPUT VOLTAGE



WARM-UP DRIFT VS TIME



DISCUSSION OF PERFORMANCE

A simplified diagram of the INA110 is shown on the first page. The design consists of the classical three operational amplifier configuration with precision FET buffers on the input. The result is an instrumentation amplifier with premium performance not normally found in integrated circuits.

The input section (A_1 and A_2) incorporates high performance, low bias current, and low drift amplifier circuitry. The amplifiers are connected in the noninverting configuration to provide high input impedance ($10^{12}\Omega$). Laser-trimming is used to achieve low offset voltage. Input cascoding assures low bias current and high CMR. Thin-film resistors on the integrated circuit provide excellent gain accuracy and temperature stability.

The output section (A_3) is connected in a unity-gain difference amplifier configuration. Precision matching of the four 10kΩ resistors, especially over temperature and time, assures high common-mode rejection.

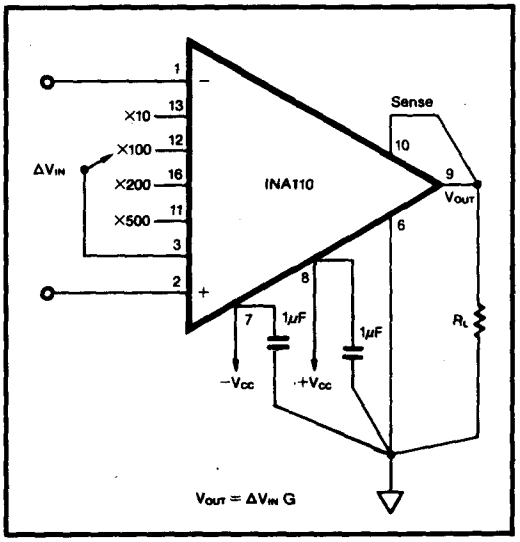


FIGURE 1. Basic Circuit Connection.

BASIC POWER SUPPLY AND SIGNAL CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. Supplies should be decoupled with 1µF tantalum capacitors as close to the amplifier as possible. To avoid gain and CMR errors introduced by the external circuit, connect grounds as indicated, being sure to minimize ground resistance. Resistance in series with the reference (pin 6) will degrade CMR. Also to maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins. The layout shown in Figure 2 is suggested for best performance.

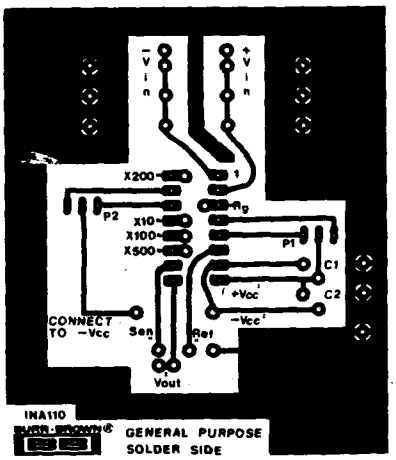
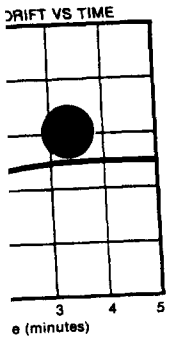
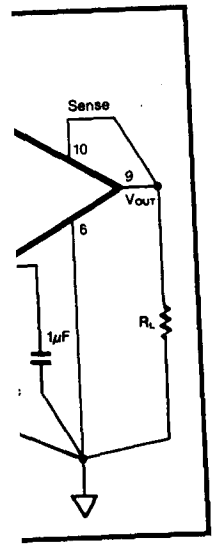


FIGURE 2. Recommended PC Board Layout for INA110.

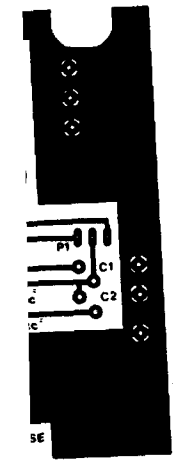
OFFSET ADJUSTMENT

Figure 3 shows the offset adjustment circuit for the INA110. Both the offset of the input stage and output stage can be adjusted separately. Notice that the offset referred to the INA110's input (RTI) is the offset of the input stage plus the offset of the output stage divided by





on.



Board Layout for

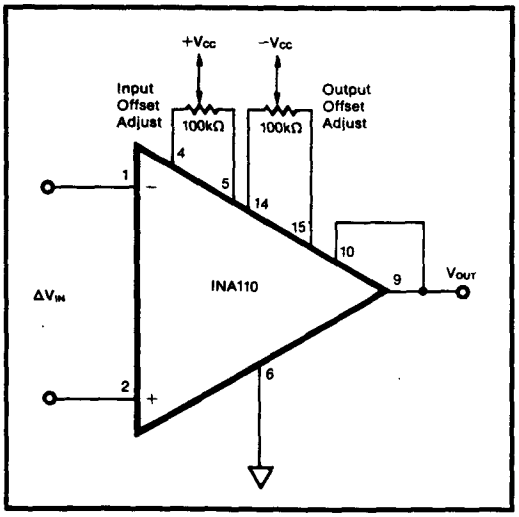


FIGURE 3. Offset Adjustment Circuit.

the gain of the input stage. This allows specification of offset independent of gain.

For systems using computer autozeroing techniques, neither offset nor offset drift are of concern. In many other applications the factory-trimmed offset gives excellent results. When greater accuracy is desired, one adjustment is usually sufficient. In high gains (>100) adjust only the input offset, and in low gains the output offset. For higher precision in all gains, both can be adjusted by first selecting high gain and adjusting input offset and then low gain and adjusting output offset. The offset adjustment will, however, add to the drift by approximately 0.33μV/°C per 100μV of input offset voltage that is adjusted. Therefore, care should be taken when considering use of adjustment.

Output offsetting can be accomplished as shown in Figure 4 by applying a voltage to the reference (pin 6)

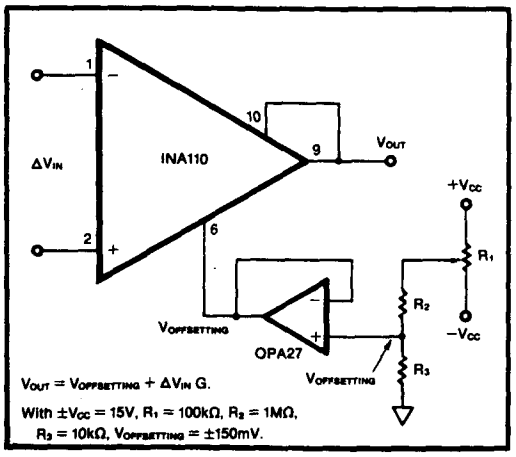


FIGURE 4. Output Offsetting.

through a buffer. This limits the resistance in series with pin 6 to minimize CMR error. Be certain to keep this resistance low. Note that the offset error can be adjusted at this reference point with no appreciable degradation in offset drift.

GAIN SELECTION

Gain selection is accomplished by strapping the appropriate pins together on the INA110. Table I shows possible gains from the internal resistors. Keep the connections as short as possible to maintain accuracy.

TABLE I. Internal Gain Connections.

Gain	Connect pin 3 to pin —	Gain Accuracy (%)	Gain Drift (ppm/°C)
The following gains have guaranteed accuracy:			
1	none	0.02	10
10	13	0.05	10
100	12	0.1	20
200	16	0.2	30
500	11	0.5	50
The following gains have typical accuracy as shown:			
300	12 & 16	0.25	10
600	11 & 12	0.25	40
700	11 & 16	2.0	40
800	11, 12, & 16	2.0	80

Gains other than 1, 10, 100, 200, and 500 can be set by adding an external resistor, R_G, between pin 3 and pins 12, 16, and 11. Gain accuracy is a function of R_G and the internal resistors which have a ±20% tolerance with 20ppm/°C drift. The equation for choosing R_G is shown below.

$$R_G = \frac{40k}{G - 1} - 50\Omega$$

Gain can also be changed in the output stage by adding resistance to the feedback loop shown in Figure 5. This is useful for increasing the total gain or reducing the input stage gain to prevent saturation of input amplifiers.

The output gain can be changed as shown in Table II. Matching of R_1 and R_3 is required to maintain high CMR. R_2 sets the gain with no effect on CMR.

TABLE II. Output Stage Gain Control.

Output Stage Gain	R_1 and R_3	R_2
2	1.2kΩ	2.74kΩ
5	1kΩ	511Ω
10	1.5kΩ	340Ω

COMMON-MODE INPUT RANGE

It is important not to exceed the input amplifiers' dynamic range (see Typical Performance Curves). The differential input signal and its associated common-mode voltage should not cause the output of A_1 and A_2 (input amplifiers) to exceed approximately ±10V with ±15V supplies or nonlinear operation will result. Such large common-mode voltages, when the INA110 is in high gain, can cause saturation of the input stage even though the differential input is very small. This can be avoided by reducing the input stage gain and increasing the output stage gain with an H pad attenuator (see Figure 5).

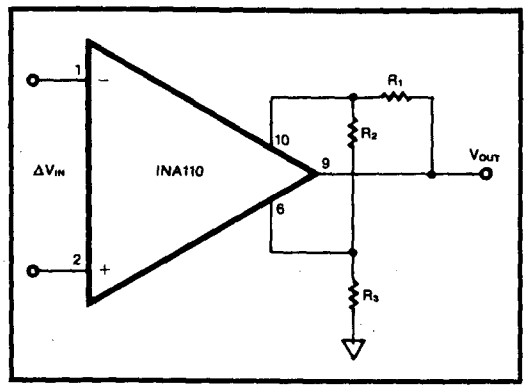


FIGURE 5. Gain Adjustment of Output Stage Using H Pad Attenuator.

OUTPUT SENSE

An output sense has been provided to allow greater accuracy in connecting the load. By attaching this feedback point to the load at the load site, IR drops due to load currents are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more current is to be supplied, a power booster can be placed within the feedback loop as shown in Figure 6. Buffer errors are minimized by the loop gain of the output amplifier.

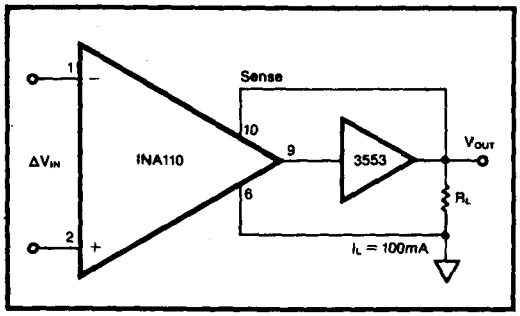


FIGURE 6. Current Boosting the Output.

LOW BIAS CURRENT OF FET INPUT ELIMINATES DC ERRORS

Because the INA110 has FET inputs, bias currents drawn through input source resistors have a negligible effect on DC accuracy. The picoamp levels produce no more than microvolts through megohm sources. Thus, input filtering and input series protection are readily achievable.

A return path for the input bias currents must always be provided to prevent charging of stray capacitance. Otherwise the output can wander and saturate. A 1MΩ to 10MΩ resistor from the input to common will return floating sources such as transformers, thermocouples, and AC-coupled inputs (see Applications section).

DYNAMIC PERFORMANCE

The INA110 is a fast-settling FET input instrumentation amplifier. Therefore, careful attention to minimize stray capacitance is necessary to achieve specified performance. High source resistance will interact with input capacitance to reduce the overall bandwidth. Also, to maintain stability, avoid capacitance from the output to the gain set, offset adjust, and input pins (see Figure 2 for PC board layout).

When using high source resistance (>20kΩ) in the positive input only, bypass it to ground with at least 50pF to maintain stability.

The INA110 is designed for fast settling with easy gain selection. It has especially excellent settling in high gain. It can also be used in fast-settling unity-gain applications. As with all such amplifiers, the INA110 does exhibit signficant gain peaking when set to a gain of 1. It is, however, unconditionally stable. The gain peaking can be cancelled by band-limiting the negative input to 400kHz with a simple external RC circuit for applications requiring flat response.

Another distinct advantage of the INA110 is the high frequency CMR response. High frequency noise and sharp common-mode transients will be rejected. To preserve AC CMR, be sure to minimize stray capacitance on the input lines. Matching the RCs in the two inputs will help to maintain high AC CMR.

APPLICATIONS

In addition to general purpose uses, the INA110 is designed to accurately handle two important and demanding applications: (1) inputs with high source impedances such as capacitance/crystal/photodetector sensors and low-pass filters and series-input protection devices, and (2) rapid-scanning data acquisition systems requiring fast settling time. Because the user has access to the output sense, current sources can also be constructed using a minimum of external components. Figures 7 through 24 show application circuits.